AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) A memory module for storing data, including:

a) a first circuit board having a plurality of electrical terminals for sending data to and receiving data from ~~interfacing with~~ a second circuit board;

b) a volatile memory device mounted on the first circuit board; and

c) a radio transmitter mounted on the first circuit board, the radio transmitter operable to transmit information related to the number of rows on the memory module and the number of columns on the memory module to a radio receiver mounted on the second circuit board thereby enabling a device on the second circuit board to utilize said information to write data to the volatile memory device via the plurality of terminals.

2. (Currently amended) A memory module for storing data, comprising:

a) a first circuit board having a plurality of electrical terminals for sending data to and receiving data from ~~interfacing with~~ a second circuit board;

b) a volatile memory device mounted on the first circuit board;

c) a non-volatile memory device mounted on the first circuit board, the non-volatile memory device storing information related to the number of rows on the memory module and the number of columns on the memory module; and

d) a radio transmitter mounted on the first circuit board, the radio transmitter operable to receive said information from the non-volatile memory device and transmit said information to a radio receiver mounted on the second circuit board thereby enabling a device on the

second circuit board to utilize said information to write data to the volatile memory device via the plurality of terminals.

3. (Original) The memory module of claim 2, wherein the volatile memory device is a dynamic random access memory (DRAM) device.

4. (Original) The memory module of claim 2, wherein the volatile memory device is a synchronous dynamic random access memory (SDRAM) device.

5. (Original) The memory module of claim 2, wherein the non-volatile memory device is an electrically programmable read only memory (EPROM).

6. (Original) The memory module of claim 2, wherein the non-volatile memory device is an electrically erasable programmable read only memory (EEPROM).

7. (Original) The memory module of claim 2, wherein the non-volatile memory device is a serial electrically erasable programmable read only memory (SEEPROM).

8. (Original) The memory module of claim 2, wherein the non-volatile memory is connected to the radio transmitter via an I^2C bus.

9. (Original) The memory module of claim 2, wherein the radio transmitter is a radio transceiver.

10. (Previously presented) The memory module of claim 9, further comprising:

e) a processor that is mounted on the first circuit board, the processor being operable to determine the physical location of the memory module with respect to the second circuit board by determining the signal strength of a radio signal received from a second radio transmitter.

11. (Previously presented) The memory module of claim 9, further comprising:

e) a processor that is mounted on the first circuit board, the processor being operable to determine the physical location of the memory module with respect to the second circuit board by determining the propagation delay of a radio signal received from a second radio transmitter.

12. (Previously presented) The memory module of claim 9, wherein the radio transceiver is operable to receive radio signals from a second radio transmitter and a third radio transmitter.

13. (Previously presented) The memory module of claim 9, further comprising:

e) a processor that is mounted on the first circuit board, the processor being operable to determine the physical location of the memory module with respect to the second circuit board by determining the signal strength of a radio signal received from a second radio

transmitter and the signal strength of a radio signal received from a third radio transmitter.

14. (Previously presented) The memory module of claim 9, further comprising:

e) a processor that is mounted on the first circuit board, the processor being operable to determine the signal strength of a radio signal received from a second radio transmitter, the signal strength of a radio signal received from a third radio transmitter, and the physical location of the memory module with respect to the second circuit board based upon the determined signal strengths.

15. (Previously presented) The memory module of claim 9, further comprising:

e) a processor that is mounted on the first circuit board, the processor being operable to determine the physical location of the memory module with respect to the second circuit board by determining the propagation delay of a radio signal received from a second radio transmitter and the propagation delay of a radio signal received from a third radio transmitter.

16. (Previously presented) The memory module of claim 9, further comprising:

e) a processor that is mounted on the first circuit board, the processor being operable to determine the propagation delay of a radio signal received from a second radio transmitter, the propagation delay of a radio signal received from a third radio transmitter, and the physical location of the memory module with respect to the second circuit board based upon the determined signal propagation delays.

17. (Previously presented) The memory module of claim 9, further comprising:

e) a processor that is mounted on the first circuit board, the processor being operable to determine the signal strength and the propagation delay of a radio signal received from a second radio transmitter and the signal strength and the propagation delay of a radio signal received from a third radio transmitter.

18. (Previously presented) The memory module of claim 9, further comprising:

e) a processor that is mounted on the first circuit board, the processor being operable to determine the signal strength and the propagation delay of a radio signal received from a second radio transmitter, the signal strength and the propagation delay of a radio signal received from a third radio transmitter, and the location of the memory module with respect to the second circuit board based upon the determined signal strengths and propagation delays.

19. (Currently amended) A memory module for storing data, comprising:

a) a first circuit board having a plurality of electrical terminals for sending data to and receiving data from ~~interfacing with~~ a second circuit board;

b) a volatile memory device mounted on the first circuit board; and

c) a radio transmitter mounted on the first circuit board, the radio transmitter including a non-volatile memory cell for storing information related to the number of rows on the memory module and the number of columns on the memory module, the radio transmitter being operable to transmit said information to a radio receiver mounted on the second circuit board thereby enabling a device on the second circuit board to utilize said information to

write data to the volatile memory device via the plurality of terminals.

20. (Original) The memory module of claim 19, wherein the radio transmitter is a radio transceiver.

21. (Previously presented) The memory module of claim 20, further comprising:

d) a processor that is mounted on the first circuit board, the processor being operable to determine the signal strength of a radio signal received from a radio transmitter.

22. (Previously presented) The memory module of claim 20, further comprising:

d) a processor that is mounted on the first circuit board, the processor being operable to determine the propagation delay of a radio signal received from a second radio transmitter.

23. (Previously presented) The memory module of claim 20, wherein the radio transceiver is operable to receive radio signals from a second radio transmitter and a third radio transmitter.

24. (Previously presented) The memory module of claim 20, further comprising:

d) a processor that is operable to determine the signal strength of a radio signal received from a second radio transmitter and the signal strength of a radio signal received from a third radio transmitter.

25. (Previously presented) The memory module of claim 20, further comprising:

d) a processor that is operable to determine the signal strength of a radio signal received from a second radio transmitter, the signal strength of a radio signal received from a third radio transmitter, and the physical location of the memory module with respect to the second circuit board based upon the determined signal strengths.

26. (Previously presented) The memory module of claim 20, further comprising:

d) a processor that is operable to determine the propagation delay of a radio signal received from a second radio transmitter and the propagation delay of a radio signal received from a third radio transmitter.

27. (Previously presented) The memory module of claim 20, further comprising:

d) a processor that is operable to determine the propagation delay of a radio signal received from a second radio transmitter, the propagation delay of a radio signal received from a third radio transmitter, and the physical location of the memory module with respect to the second circuit board based upon the determined signal propagation delays.

28. (Previously presented) The memory module of claim 20, further comprising:

d) a processor that is operable to determine the signal strength and the propagation delay of a radio signal received from a second radio transmitter and the signal strength and the propagation delay of a radio signal received from a third radio transmitter.

29. (Previously presented) The memory module of claim 20, further comprising:

d) a processor that is operable to determine the signal strength and the propagation delay of a radio signal received from a second radio transmitter, the signal strength and the propagation delay of a radio signal received from a third radio transmitter, and the physical location of the memory module with respect to the second circuit board based upon the determined signal strengths and propagation delays.

30. (Currently amended) A computer system for processing data, comprising:

a) a memory module for storing data, including:

1) a first circuit board having a plurality of electrical terminals;

2) a volatile memory device mounted on the circuit board;

3) a radio transmitter mounted on the first circuit board, the radio transmitter operable to transmit information related to the number of rows on the memory module and the number of columns on the memory module; and

b) a second circuit board physically coupled to a radio receiver that is operable to receive the information from the radio transmitter, the radio receiver operable to provide the received information to a device on the second circuit board thereby enabling a device on the second circuit board to utilize said information to write data to the volatile memory device <u>via the plurality of electrical terminals,</u>

<u>wherein the first circuit board is operable to send data to and receive data from the second circuit board via the plurality of electrical terminals.</u>

31. (Original) The computer system of claim 30 wherein the radio receiver is coupled to a processor that is operable to determine the signal strength of a radio signal transmitted from the radio transmitter.

32. (Original) The computer system of claim 30, wherein the radio receiver is coupled to a processor that is operable to determine the propagation delay of a radio signal transmitted from the radio transmitter.

33. (Original) The computer system of claim 30, wherein the radio receiver is coupled to a processor that is operable to determine the signal strength and the propagation delay of a radio signal transmitted from the radio transmitter.

34. (Previously presented) The computer system of claim 30, wherein the radio receiver is coupled to a processor that is operable to determine the physical location of the memory module with respect to the second circuit board.

35. (Canceled)

36. (Canceled)

37. (Canceled)

38. (Canceled)

39. (Canceled)

40. (Currently amended) A method of determining the number of columns of a memory module and the number of rows of a memory module in a computer system, comprising:

a) installing a memory module on a first circuit board, the memory module including a volatile memory device and a plurality of terminals for sending data to and receiving data from a second circuit board;

b) transmitting information relating to the number of columns of a memory module and information relating to the number of rows of a memory module from a radio transmitter that is mounted on the first circuit board of the memory module to a radio receiver physically coupled to the ~~a~~ second circuit board;

c) receiving the memory module information with the radio receiver; and

d) utilizing the received memory module information to determine the number of columns of a memory module and the number of rows of a memory module and utilizing the number of columns and the number of rows to write data to a volatile memory device on the memory module via the plurality of terminals.

41. (Previously presented)The method of claim 40, further comprising:

e) using the received memory module information to configure a memory controller.

42. (Canceled).

43. (Canceled)

44. (Previously presented) A method of determining the location of a memory module that is installed in a first circuit board with respect to the first circuit board, comprising:

a) determining the signal strength of a radio signal; and

b) based upon the determined signal strength, determining the physical location of the memory module with respect to the first circuit board.

45. (Previously presented) A method of determining the location of a memory module that is installed in a first circuit board with respect to the first circuit board, comprising:

a) determining the signal strength of a first radio signal;

b) determining the signal strength of a second radio signal; and

c) based upon the determined signal strengths, determining the physical location of the memory module with respect to the first circuit board.

46. (Previously presented) A method of determining the location of a memory module that is installed in a first circuit board with respect to the first circuit board, comprising:

a) determining the propagation delay of a radio signal; and

b) based upon the determined propagation delay, determining the physical location of the memory module with respect to the first circuit board.

47. (Previously presented) A method of determining the location of a memory module that is installed in a first circuit board with respect to the first circuit board, comprising:

a) determining the propagation delay of a first radio signal;

b) determining the propagation delay of a second radio signal; and

c) based upon the determined propagation delays, determining the physical location of the memory module with respect to the first circuit board.

48. (Original) The memory module of claim 1, wherein the radio transmitter is operable to transmit information that indicates that the memory module failed a test.

49. (Original) The memory module of claim 1, wherein the radio transmitter is operable to transmit information that indicates that the memory module failed self-test.

50. (Original) The memory module of claim 1, wherein the radio transmitter is operable to transmit information that indicates that the memory module failed an interconnect test.

51. (Original) The memory module of claim 1, wherein the radio transmitter is operable to transmit information that indicates that the memory module failed an error correction code test.